REMARKS

Claims 1-63 are pending. Claims 28-31 and 58-63 have been examined, and the remaining claims have been withdrawn from consideration. All examined claims have been rejected.

Specification

In accordance with the Examiner's request, Applicant has amended the specification to fill in information in the blanks on page 10, line 36, and page 17, line 2.

Claim Rejections - 35 U.S.C. § 112

Claims 28-31 and 58-63 are rejected under 35 U.S.C. § 112, second paragraph, as being incomplete. Applicant has hereby amended the claims to make them more complete. Withdrawal of this rejection is therefore respectfully requested.

Claim Rejections - 35 U.S.C. §§ 102 and 103

Claims 28 and 58 are rejected under 35 U.S.C. § 102(b) as being anticipated by Critchlow (U.S. Patent No. 5,276,706) and also by Davidovoci (U.S. Patent No. 5,802,102). Claims 28, 58-61, and 63 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim et al. (U.S. Patent No. 6,219,374) in view of Critchlow. Applicant respectfully traverses these rejections for the reasons set forth below.

The present invention is directed to a configurable receiver for a CDMA system, which has an RF/IF stage 102 for receiving an analog signal, an analog-to-digital converter 104 for converting the analog signal to a digital signal, a chip-matched filter 108 for filtering the digital signal, and at least one configurable digital coherent demodulator system 110 for feed forward phase correcting the filtered digital signal. The invention also relates to a method of processing data using this configurable CDMA receiver. Because the phase error is corrected in the forward direction, the phase of the data signal is corrected in real time. Thus, the present invention provides an advantage over conventional systems using feedback timing wherein data signals are corrected for a past phase error.

Critchlow is directed a system and method for frequency acquisition in digital communication systems. The Examiner alleges that Critchlow teaches a means for receiving an analog signal at an RF stage 16, 18, an analog-to-digital converter 18, a means for filtering the digital signal using a matched filter 24, and a demodulator for feed forward phase correcting the filtered digital signal with a correcting signal 48. See Critchlow, Fig. 1.

Contrary to the Examiner's position, Critchlow does not teach the claimed configurable digital coherent demodulator system for feed forward phase correcting a filtered digital signal. As its names implies, a feed forward signal is fed forward, not backward. The alleged correction signal 48 to which the Examiner refers is fed backward in the system from the parabolic interpreter 46 to the down converter 16 through the voltage controlled local oscillator 49, and thus can not be a feed forward signal. Thus, claims 28 and 58 are patentable over Pritchard for at least this reason.

Davidovici is directed to a programmable matched filter which despreads a pilot-chip-code-sequence signal and a message-chip-code-sequence signal. The Examiner directs Applicant to Fig. 1, which the Examiner alleges teaches a means for receiving an analog signal at an RF/IF stage 31-34, an analog-to-digital converter 33, 34, a filter for filtering the digital signal 35, 37 to obtain a complex signal, and a demodulator 41, 46, 38, 39 for processing the complex signal output from the filters 35, 37 using correction signals from MF controller 46.

Contrary to the Examiner's position, Davidovici does not teach a configurable digital coherent demodulator system for feed forward phase correcting a filtered digital signal. Assuming for the sake of argument that the MF controller 46 outputs correction signals as the Examiner suggests, these signals are fed backward in the demodulator to various components rather than forward. These signals therefore can not be feed forward signals. Thus claims 28 and 58 are patentable over Davidovici for at least this reason.

Kim is directed to a coherent dual channel quadrature phase shift keying transceiver using pilot symbols in a code division multiple access system. The Examiner directs Applicant to Fig. 3 and alleges that Kim teaches a means for receiving an analog signal at an RF/IF stage 301, a filter for filtering the analog signal using a matched filter 303, 304 to obtain a complex signal, and a demodulator 305-318 for processing the complex signal output from the filters 303,

304 using correction signals from the channel estimators 317, 318. The Examiner admits that Kim does not teach an analog-to-digital-converter. The Examiner attempts to make up for this deficiency by stating that Kim does not disclose whether or not the matched filter is a digital filter, and then cites Critchlow as teaching a digital matched filter 24, which would necessarily need a digital-to-analog converter to first convert the analog signal to digital format.

Contrary to the Examiner's position, there is no disclosure or suggestion in Kim that the channel estimators 317, 318 produce correction signals used by a demodulator to feed forward phase correct a filtered digital signal, as required by the claims of the present invention. Kim does disclose in column 4, lines 59-64, that the channel estimators 317, 318 produce signals used in the channel estimation values upon data demodulation. But these values are fed backward to mixers 307-310. There is no disclosure that these values are fed forward to correct a filtered digital signal, as required by the claims of the present invention. Moreover, Critchlow does not make up for this deficiency by teaching this feature for the reasons discussed above. Thus the claims are patentable over Kim in view of Critchlow for at least this reason.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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